MASTER SYLLABUS

ELEC 355 – EMBEDDED ELECTRONICS

Created by: Dr. Shahrokh Sani

SCHOOL OF ENGINEERING TECHNOLOGY
ELECTRICAL ENGINEERING TECHNOLOGY & ENGINEERING SCIENCE DEPARTMENT

Fall- 2021

A. **TITLE**: EMBEDDED ELECTRONICS

B. **COURSE NUMBER:** ELEC 355

C. **CREDIT HOURS (Hours of Lecture, Laboratory, Recitation, Tutorial, Activity):**

 # Credit Hours: 3
 # Lecture Hours per Week: 2 per week
 # Lab Hours per Week: 2 per week
Other per Week:

Course Length (# of Weeks): 15 weeks

D. WRITING INTENSIVE COURSE: No

E. GER CATEGORY: None

F. SEMESTER(S) OFFERED: Fall/Spring

G. COURSE DESCRIPTION: This course is designed to give students theoretical and hands-on experience in Field Programmable Gate Array (FPGA) and Very High-Speed Integrated Circuit Hardware Description Language (VHDL). The course covers the concept and architecture of Programmable Logic Device. The graphic editor of Altera's Quartus Design software and VHDL text editor are used to define digital logic to FPGA.

H. PRE-REQUISITES/CO-REQUISITES:

a. Pre-requisite(s): ELEC 165 (Digital Fundamentals & Systems), ELEC 166 (Digital Fundamentals & Systems Laboratory) and MATH 123 (Pre-Calculus Algebra) or permission of the instructor.
b. Co-requisite(s): None
c. Pre- or co-requisite(s):

I. STUDENT LEARNING OUTCOMES:

Course Student Learning Outcome [SLO]	ABET Student Outcomes (1-5)	***ISLO***
a. Solve problems that arise with Programmable Logic Device (PLD).	1. An ability to apply knowledge, techniques, skills and modern tools of mathematics, science, engineering, and technology to solve broadly defined engineering problems appropriate to the discipline.	5. Industry, Professional, Discipline-Specific Knowledge and Skills
b. Design flow and simulation processes associated with a design using VHDL and synthesizing it on FPGAs.	1. An ability to apply knowledge, techniques, skills and modern tools of mathematics, science, engineering, and technology to solve broadly defined engineering problems appropriate to the discipline.	5. Industry, Professional, Discipline-Specific Knowledge and Skills

c. Work with modern FPGA design tools including Intel (Altera) FPGAs	1. An ability to apply knowledge, techniques, skills and modern tools of mathematics, science, engineering, and technology to solve broadly defined engineering problems appropriate to the discipline.	5. Industry, Professional, Discipline-Specific Knowledge and Skills
d. Construct and test digital circuits using VHDL code.	4. An ability to conduct standard tests, measurements, and experiments and to analyze and interpret the result to improve processes.	2. Critical Thinking – [PS]

KEY	**Institutional Student Learning Outcomes [ISLO 1 – 5]**
ISLO #	**ISLO & Subsets**
1	**Communication Skills** Oral [O], Written [W]
2	**Critical Thinking** *Critical Analysis [CA] , Inquiry & Analysis [IA] , Problem Solving [PS]*
3	**Foundational Skills** *Information Management [IM], Quantitative Lit,/Reasoning [QTR]*
4	**Social Responsibility** *Ethical Reasoning [ER], Global Learning [GL], Intercultural Knowledge [IK], Teamwork [T]*
5	**Industry, Professional, Discipline Specific Knowledge and Skills**

J. APPLIED LEARNING COMPONENT: **Yes__√____ No_____**

If Yes, select one or more of the following categories:

Classroom/Lab_√__
Internship___
Clinical Practicum___
Practicum___
Service Learning___
Community Service___
Civic Engagement___
Creative Works/Senior Project___
Research___
Entrepreneurship___
(program, class, project)

K. **TEXTS:** Digital Electronics: A Practical Approach with VHDL 9th Edition by William Kleitz. ISBN-10: 0132543036

L. **REFERENCES:** The Design Warrior's Guide to FPGAs, Devices, Tools and Flows, Clive "Max" Maxfield, ISBN: 0-7506-7604-3

M. **EQUIPMENT:** Altera DE2-115 Development and Education Board.

N. **GRADING METHOD:** A-F

O. **SUGGESTED MEASUREMENT CRITERIA/METHODS:**

- Exams
- Projects
- Participation
- Presentation

P. **DETAILED COURSE OUTLINE:**

I. Programable Logic Devices (PLD)
   A. PLD Design Flow
   B. PLD Architecture
   C. Using PLDs to solve basic logic design

II. Field Programmable Gate Array (FPGA)
   A. Altera's Quartus II design and simulation software
   B. FPGA applications with VHDL
   C. FPGA applications with LPMs
   D. FPGA electrical characteristics
   E. Schematic Design for Intel (Altera) FPGAs
   F. Waveform Simulation for Intel (Altera) FPGAs
   G. VHDL Program for Intel (Altera) FPGAs

III. Boolean Algebra and Reduction Techniques
   A. Using FPGA to Solve Basic Logic Designs.
   B. Entering Truth Tables Using VHDL Vector Signals.

IV. Exclusive OR and Exclusive NOR Gates
   A. FPGA Parallel Binary Comparator
   B. FPGA Controlled Inverter

V. Arithmetic Operations and Circuits
   A. Library of Parameterized Modules (LPM)
   B. 8-Bit Binary Adder/Subtractor
   C. BCD Adder
   D. LPM Adder/Subtractor

VI. Code Converters, Multiplexers, and Demultiplexers
   A. Decoders and Multiplexer Implementation in VHDL
   B. Decoders and Multiplexer Using LPMs
   C. LPM Comparator

VII. Flip-Flops and Registers
   A. VHDL Description of a D Flip-Flop
   B. VHDL Description of a J-K Flip-Flop
   C. LPM Flip-Flop

VIII. Counter Circuits and VHDL State Machines
   A. VHDL Description of a 16-Bits Up Counter
   B. VHDL Description of the Seven-Segment Decoder
   C. LPM Counter
   D. Implementing State Machines in VHDL

IX. Other Topics: As Defined by the Instructor (The topics on FPGA applications are strongly recommended)

Q. <u>LABORATORY OUTLINE</u>:

A. Using FPGA to Solve Basic Logic Designs.
B. Schematic Design for Intel (Altera) FPGAs.
C. Waveform Simulation for Intel (Altera) FPGAs.
D. VHDL Program for Intel (Altera) FPGAs.
E. Entering Truth Tables Using VHDL Vector Signals.
F. VHDL Description of Adders.
G. Decoders and Multiplexer Implementation in VHDL.
H. VHDL FPGA Design Using LPMs.
I. VHDL Description of Flip-Flops.
J. VHDL Description of Counters.
K. VHDL Description of Seven Segment Decoder.
L. Implementing State Machines in VHDL.
M. VHDL Description of Shift Registers.
N. VHDL Components and Instantiations