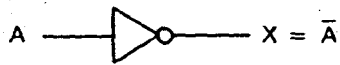
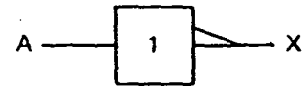


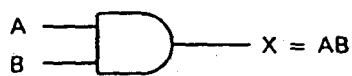
Inverter:



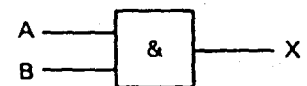
A	X
0	1
1	0



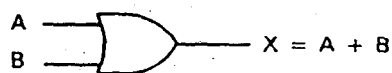
AND:



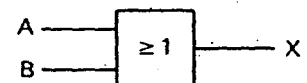
A	B	X
0	0	0
0	1	0
1	0	0
1	1	1



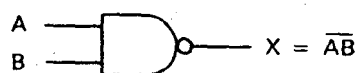
OR:



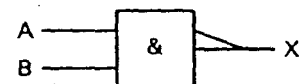
A	B	X
0	0	0
0	1	1
1	0	1
1	1	1



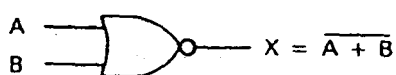
NAND:



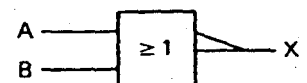
A	B	X
0	0	1
0	1	1
1	0	1
1	1	0



NOR:



A	B	X
0	0	1
0	1	0
1	0	0
1	1	0



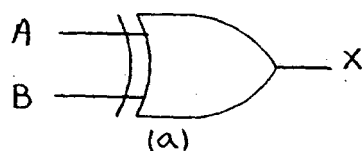
(a)

(b)

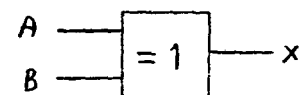
(c)

Summary of logic gates: (a) traditional logic symbols with Boolean equation; (b) truth tables; (c) IEEE/IEC standard logic symbols.

EXCLUSIVE OR:



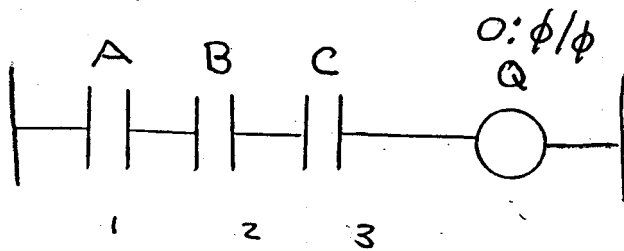
A	B	X
0	0	0
0	1	1
1	0	1
1	1	0



(b)

(c)

AND



$$A = I: \phi/1$$

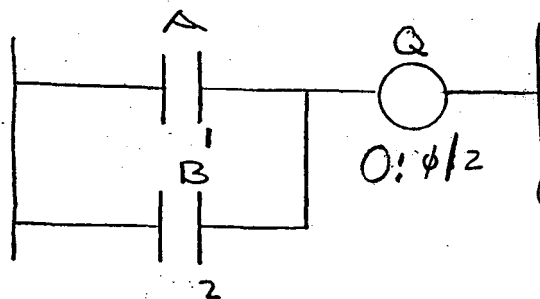
$$B = I: \phi/2$$

$$C = I: \phi/3$$

$$Q = A \cdot B \cdot C$$

$$O: \phi/\phi = I: \phi/1 \cdot I: \phi/2 \cdot I: \phi/3$$

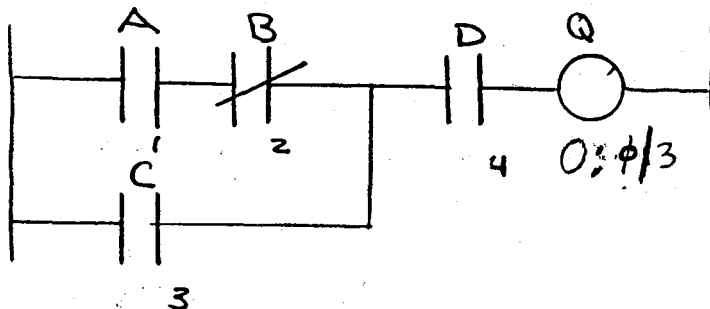
OR



$$Q = A + B$$

$$O: \phi/2 = I: \phi/1 + I: \phi/2$$

COMPLEX EXPRESSION



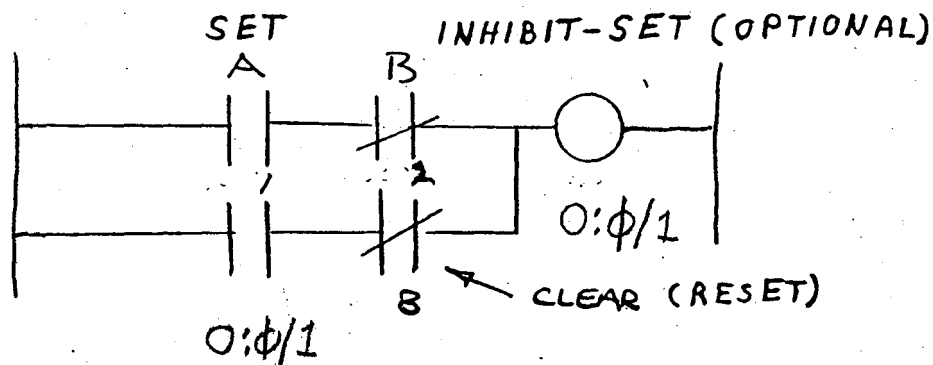
$$D = I: \phi/4$$

$$Q = [(A \cdot \bar{B}) + C] \cdot D$$

$$O/3 = ((I: \phi/1 \cdot \overline{I: \phi/2}) + I: \phi/3) \cdot I: \phi/4$$

LOGIC

CATCH #1

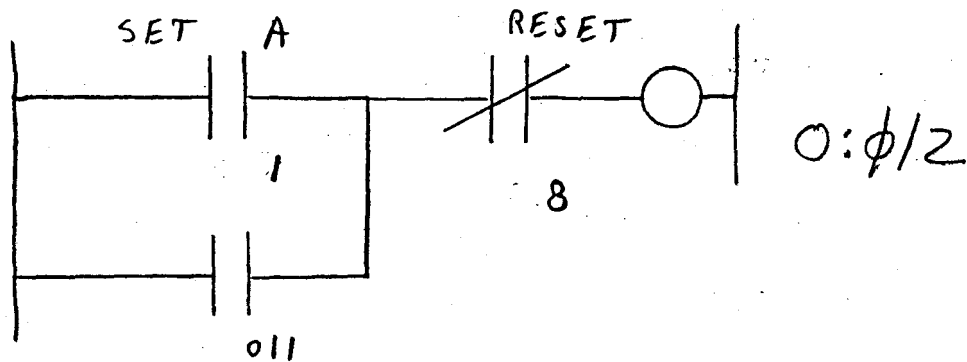


$$Q = [A + B] \cdot C + D \cdot E$$

$$\begin{aligned} A &= I:\phi/1 \\ B &= I:\phi/2 \\ C &= I:\phi/3 \\ D &= I:\phi/4 \end{aligned}$$

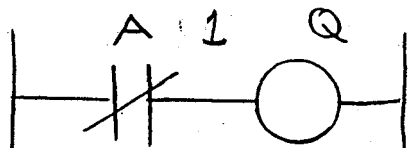
IMPLEMENT THE ABOVE EXPRESSION

LATCH #2



LOGIC

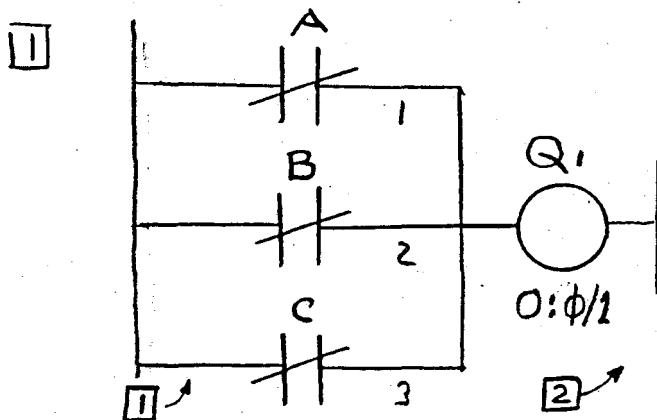
NOT



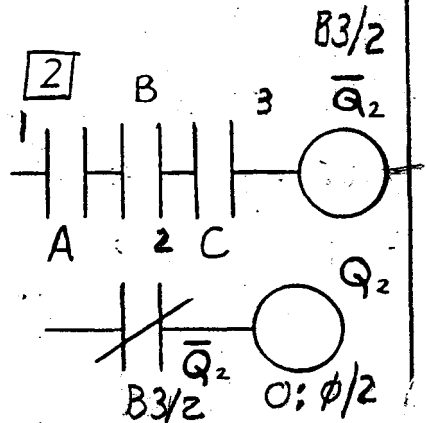
$$Q = \overline{A}$$

$$Q = 0: \phi/2 = \overline{1: \phi/1}$$

NAND



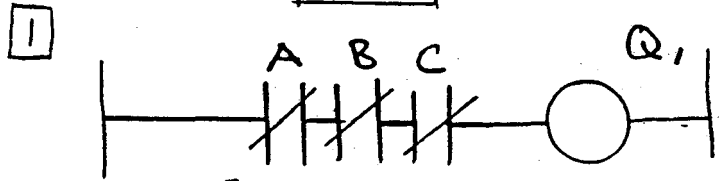
$$Q_1 = \overline{A + B + C} = \overline{A \cdot B \cdot C} = Q_2$$



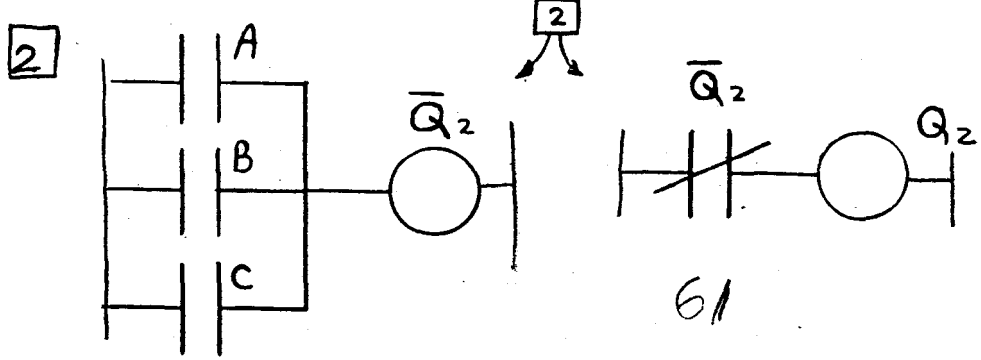
$$B3/2 = 1: \phi/1 \cdot 1: \phi/2 \cdot 1: \phi/3$$

$$0: \phi/2 = \overline{B3/2}$$

NOR



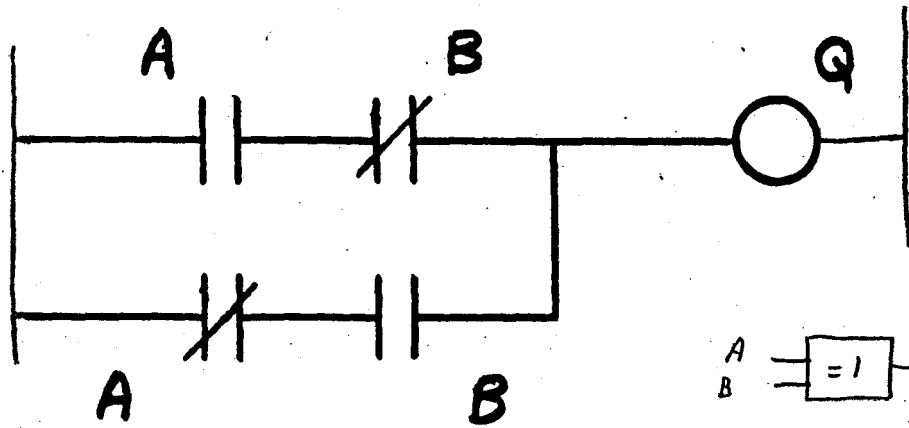
$$Q_1 = \overline{A \cdot B \cdot C} = \overline{A + B + C} = Q_2$$



LOGIC

XOR

EXCLUSIVE "OR"

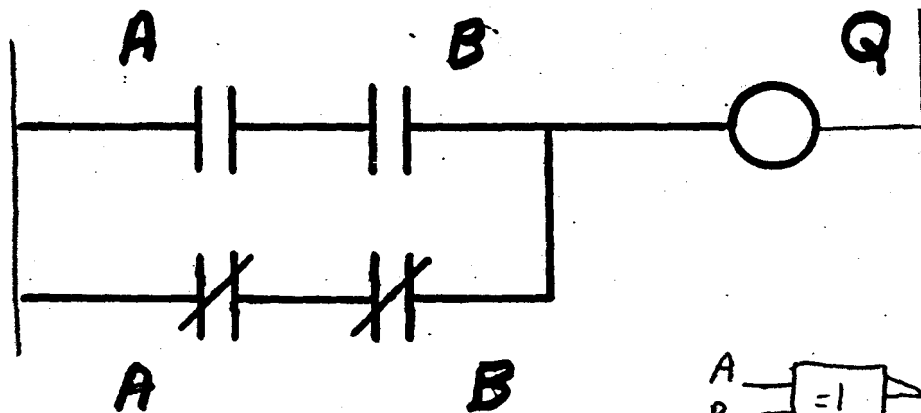


$$Q = A \cdot \bar{B} + \bar{A} \cdot B = A \oplus B$$

$$= \overline{A \odot B}$$

XNOR

EXCLUSIVE "NOR"



$$Q = A \cdot B + \bar{A} \cdot \bar{B} = \overline{A \oplus B}$$

$$= A \odot B$$